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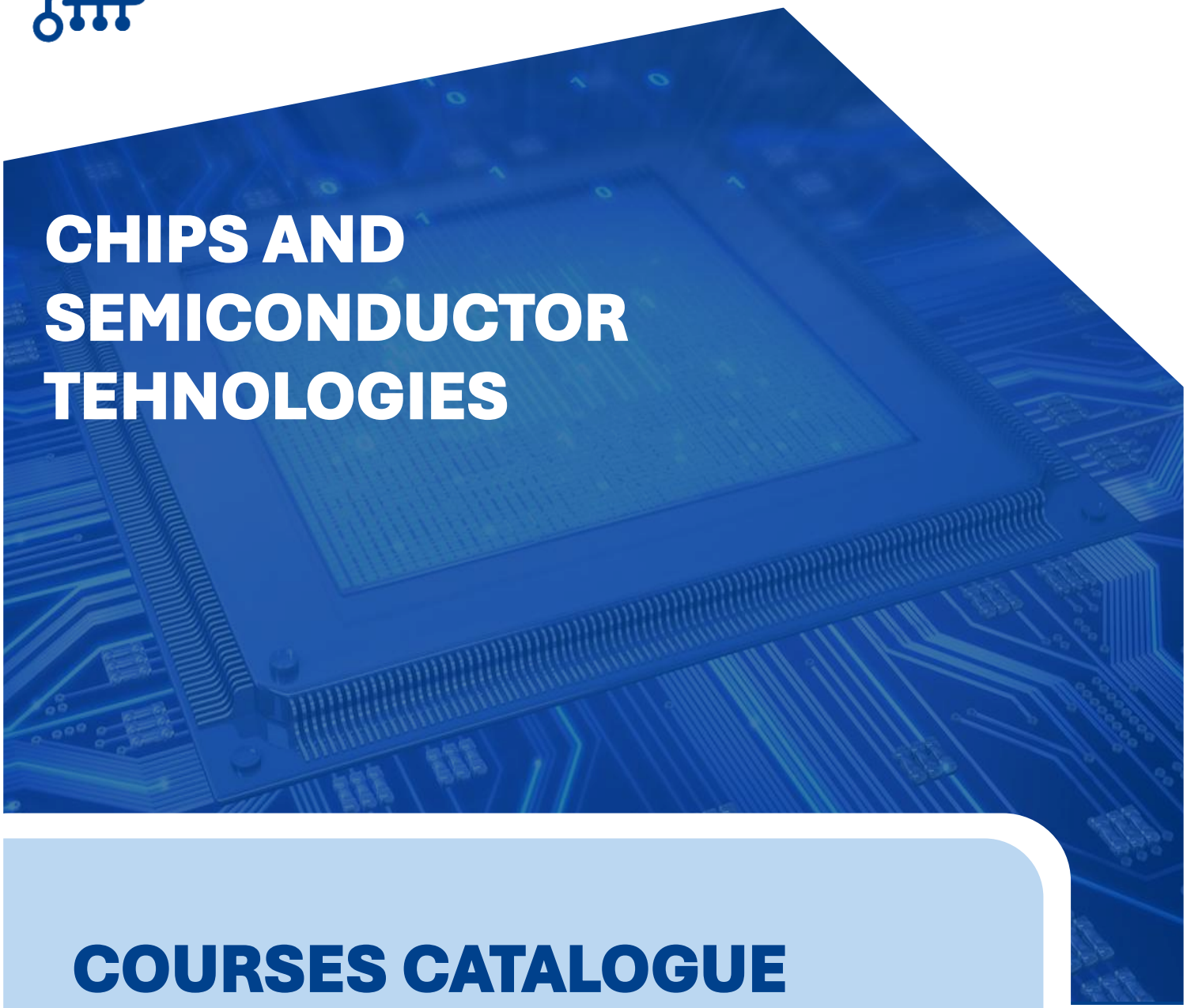

CHIPS AND SEMICONDUCTOR TEHNOLOGIES

COURSES CATALOGUE

Version 1.0

UNIVERSITY OF LJUBLJANA | FE Faculty of Electrical Engineering

UNIVERSITY OF LJUBLJANA | FRI Faculty of Computer and Information Science

University of Maribor
Faculty of Electrical Engineering

Institut "Jožef Stefan" Ljubljana, Slovenija

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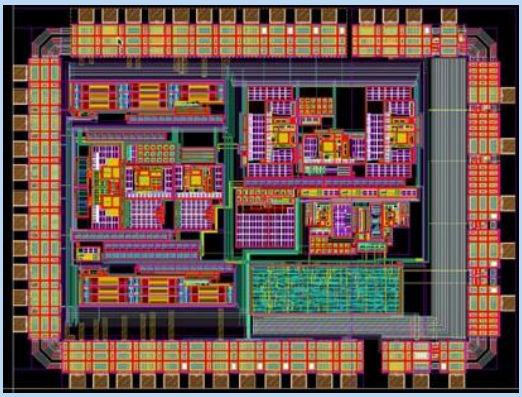
Slovenian Competence Center on Chips and Semiconductor Technologies

Courses Catalogue v1.0

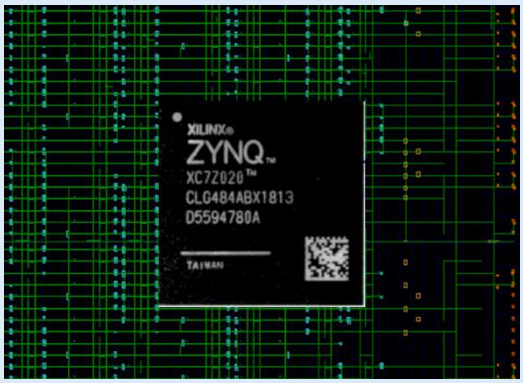
12.12.2025

COURSES AREAS

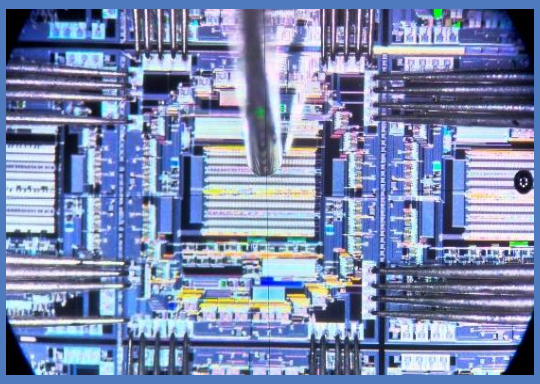
ELECTRONIC CHIPS - ASIC



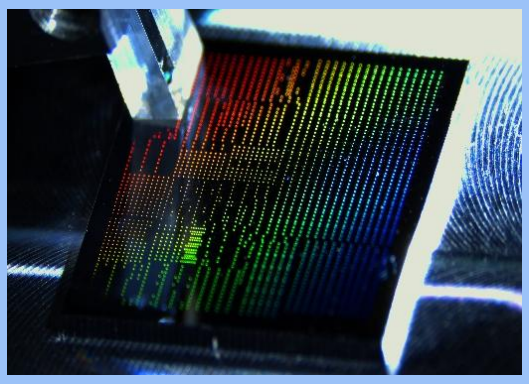
ELECTRONIC CHIPS – FPGA



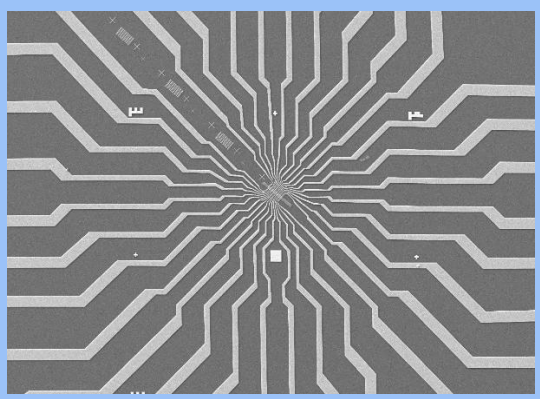
ELECTRONIC CHIPS – OTHERS



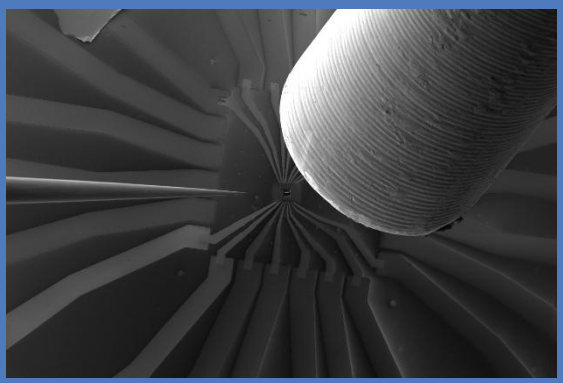
PHOTONIC CHIPS



QUANTUM CHIPS



SEMICONDUCTOR TEHNOLOGIES AND OTHER TOPICS



ABOUT THE CATALOGUE

Slovenian Competence Centre on Chips and Semiconductor Technologies – KC Chip.si aims to provide high-quality professional training courses for experts from companies, students and other interested stakeholders from the filed of chips and semiconductors.

We prepared a catalogue with short descriptions of our **50 proposed courses**. We hope and believe that this education offer will contribute to boost up-skilling and re-skilling of experts and young talents, initiating new ideas, breakthroughs and innovations in this strategic filed of chips and semiconductors.

The CC Chip.si team

University of Ljubljana, Faculty of Electrical Engineering – UL FE
University of Ljubljana, Faculty of Computer and Information Science – UL FRI
University of Maribor, Faculty of Electrical Engineering – UM FERI
University of Nova Gorica – UNG
Jožef Stefan Institute – IJS
Centre of Excellence for Nanoscience and Nanotechnology Ljubljana – NANO

CONTENT

ELECTRONIC CHIPS - ASIC 7

1. ASIC basics 7
2. ASIC specific 7
3. ASIC seminar 7
4. ASIC design/verification - course 7
5. ASIC design/verification - internship 7
6. ASIC System on Chip Design 1 - Technologies and EDA tools 7
7. ASIC System on Chip Design 2 - Analog integrated circuits and systems 8
8. ASIC System on Chip Design 3 - Analog-to-Digital and Digital-to-Analog convertors 8
9. ASIC System on Chip Design 4 - Practical workshop 8

ELECTRONIC CHIPS - FPGA 9

10. High-Level FPGA Design 9
11. FPGA-based Signal Aquisition 9
12. FPGA System on Chip Design 9
13. Zynq FPGA System on Chip Design 9
14. Ultra-fast neural network implementation on FPGA 9
15. Vitis AI - Neural networks on Xilinx FPGA accelerators 10
16. FPGAs for High Performance Computing 10
17. FPGA design development with open-source EDA 10

ELECTRONIC CHIPS - OTHERS 11

18. Wafer Test and Characterization 11
19. On Chip Die measurements 11
20. RISC-V bare metal programming 11
21. RISC-V on FPGA 11
22. Organic semiconductors and devices 12
23. Two-dimensional semiconductors and devices 12
24. OpenEDA - OpenLane DesignFlow 12
25. Computer assisted circuit assembly (OpenEDA, ML/AI in chip design) 12

26. Basics of Chisel Hardware Construction Language 13
27. Open source tools for schematic entry and circuit simulation (OpenEDA, ASIC design) 13
28. TCL scripting 13
29. EU level Supporting development - Graduate student professional training for technological progress advancement - internship 13
PHOTONIC CHIPS 14
30. Basic course on photonic integration and PIC design 14
31. Photonic integratied circuit design 14
32. Characterization and testing of photonic chips 14
33. Seminar on photonic integrated circuits and their applications 15
34. Seminar on quantum photonic integrated circits 15
35. Introduction to planar, channel waveguides and specialty optical fibres 15
36. SiPM detector testing and usage 15
37. Solid state photodetector technology overview 15
QUANTUM CHIPS 16
38. Fundamentals of superconducting device fabrication 16
39. Characterization of superconducting devices 16
40. Cryomemory device fundamentals 16
41. Hybrid devices - fabrication, test and measurement 16
SEMICONDUCTOR TECHNOLOGIES AND OTHER TOPICS 17
42. Introduction to thin film deposition (and related processes) 17
43. Nanofabrication 17
44. Laser lithography 17
45. Hands-on training on Focused Ion Beam (FIB) 17
46. Online workshop on Focused Ion Beam (FIB) 18
47. Short course on chip-based micro and nano devices: design, manufacturing and applications 18
48. Secondary and primary school teachers - train the trainers 18
49. IPR and TT internships 18
50. Specialized training in technology transfer and IPR 19

ELECTRONIC CHIPS - ASIC

This section includes a list of courses related to electronic Application Specific Integrated Circuits – ASICs.

1. ASIC basics

One day crash course, welcome to ASICs. This perpetual one-day seminar aims to provide atendees an introduction to the world of ASICs, their construction, feasibility, and commercial aspect.
*(**Provider: IJS**, Duration: 8 hours, Level: Basic)*

2. ASIC specific

One day crash course on specific topic, elaborating deeper on design tools or concrete architectual solutions.
*(**Provider: IJS**, Duration: 8 hours, Level: Advanced)*

3. ASIC seminar

An invited seminar on selected topics provides listeners with insights from experts in the field.
*(**Provider: IJS**, Duration: 4 hours, Level: Advanced)*

4. ASIC design/verification - course

This 1-month course will provide you with the possibility to use professional tools for exercising design or testing-related tasks with the aim to improve proficiency.
*(**Provider: IJS**, Duration: 1 month - 48 hours of mentoring, Level: Intermediate)*

5. ASIC design/verification - internship

3-month training (internship) aims at providing comprehensive support to see the full cycle from conception to tape out of an ASIC. Students can use this internship to train and the results to be used in their thesis.
*(**Provider: IJS,** Duration: 3 months - 144 hours of mentoring, Level: Intermediate)*

6. ASIC System on Chip Design 1 - Technologies and EDA tools

The course will introduce mainstream integrated circuit technologies, their components and how to design ASICs using industry-standard EDA tools.
*(**Provider: UL FE**, Duration: 16 hours, Level: intermediate)*

7. ASIC System on Chip Design 2 - Analog integrated circuits and systems

The course will focus on integrated analog circuit design, we will discover different MOSFET biasing regions, and then continue to explore different amplifier topologies using MOSFET transistors, current mirrors, temperature compensation, voltage/current references, single-/multi-stage amplifier design.
*(**Provider: UL FE**, Duration: 16 hours, Level: Basic)*

8. ASIC System on Chip Design 3 - Analog-to-Digital and Digital-to-Analog convertors

The course will focus on AD and DA design. We will discover SAR, Slope, sigma-delta ADCs and also DACs design.
*(**Provider: UL FE**, Duration: 16 hours, Level: Basic)*

9. ASIC System on Chip Design 4 - Practical workshop

This course will be a hands-on workshop for designing analog and mixed-signal blocks with industry standard EDA tools.
*(**Provider: UL FE**, Duration: 16 hours, Level: Basic)*

ELECTRONIC CHIPS - FPGA

This section includes a list of courses related to Field Programmable Gate Array – FPGA chips, including their design and development.

10. High-Level FPGA Design

The course will introduce high-level digital circuit synthesis (HLS) and optimization from algorithms in the C/C++ language. It covers digital design description in programming languages, hardware-specific libraries, and design techniques. The AMD Vitis HLS development tool and AMD (Xilinx) development boards will be used for practical experiments.
*(**Provider: UL FE**, Duration: 24 hours, Level: Basic)*

11. FPGA-based Signal Aquisition

The course will focus on signal acquisition applications of FPGA devices. Topics include digital interfaces, and the design and verification of data sample storage and signal processing IP blocks in RTL design languages. The AMD Vivado design tool and RedPitaya development boards will be used for practical experiments.
*(**Provider: UL FE**, Duration: 24 hours, Level: Basic)*

12. FPGA System on Chip Design

The aim of the course is to deepen the knowledge of methods of design and testing of FPGA based System on Chip, the use of soft processing cores, communication interfaces and buses, and simultaneous design of embedded hardware and software.
*(**Provider: UM FERI**, Duration: 24 hours, Level: Intermediate)*

13. Zynq FPGA System on Chip Design

The course will present the architecture of FPGA-based system-on-chip with practical use of IP, RTL, and HLS design techniques. Introduction to CPU interfaces: AXI master and slave interfaces, custom AXI peripherals, and DMA transfer. The AMD Vitis HLS and Vivado development tools, as well as AMD (Xilinx) development boards, will be used for practical experiments.
*(**Provider: UL FE**, Duration: 24 hours, Level: Basic)*

14. Ultra-fast neural network implementation on FPGA

Ultra-fast neural network inference can be achieved by heavily quantizing and pruning a

neural network. Such neural networks, if small enough, can be implemented on FPGAs in a highly parallel fashion, without using external memory. Such implementations achieve inference latencies in the order of microseconds and are useful in some specialized applications in domains such as experimental physics (triggering system), networking (real-time intrusion detection), etc.
*(**Provider: IJS**, Duration: 24 hours, Level: Basic)*

15. Vitis AI - Neural networks on Xilinx FPGA accelerators

The course introduces Vitis AI - an AMD solution for deploying deep neural networks on AMD FPGAs. The course requires a basic understanding of neural network training. In the course, you will be introduced to the basic neural network quantization in order to develop a model suitable for a AMD Vitis AI platform, you'll learn how to develop an embedded hardware platform with AMD DPU unit, and how to implement and deploy a embedded Linux application that interacts with the neural network accelerator.
*(**Provider: IJS**, Duration: 24 hours, Level: Basic)*

16. FPGAs for High Performance Computing

At the workshop, we will demonstrate how to describe, debug, and implement application-specific accelerators on FPGA using the C/C++ language rather than hardware description languages (e.g., VHDL or Verilog). Through simple examples, you will learn how to write kernels that can be synthesised on an FPGA fabric, transfer data between the host and an FPGA board, and employ various optimization techniques to make the design more efficient in terms of speed and resource utilization. Leveraging the capabilities of high-level synthesis (HLS), we will develop an accelerator for Cholesky matrix decomposition, utilizing the C/C++ programming language, along with the OpenCL and XRT libraries for development on AMD-Xilinx FPGAs. While the workshop primarily targets AMD-Xilinx FPGA boards, the principles and insights gained can be readily applied to FPGAs from various other vendors.
*(**Provider: UL FRI** , Duration: 8 hours, Level: Intermediate)*

17. FPGA design development with open-source EDA

Open-source Electronic Design Automation (EDA) tools are becoming increasingly important in FPGA development. This course introduces F4PGA, an open-source toolchain for synthesis and bitstream generation. Through hands-on exercises, participants will design and implement digital systems such as VGA controllers and UART interfaces using SystemVerilog and synthesize them with F4PGA. The course emphasizes understanding each stage of the FPGA development cycle, from design to hardware implementation. Every participant will receive an FPGA development board, enabling direct application of concepts to real hardware.
*(**Provider: UL FRI**, Duration: 8 hours, Level: Basic and intermediate)*

ELECTRONIC CHIPS - OTHERS

This section covers various topics related to electronic chip testing, design, development, verification and others.

18. Wafer Test and Characterization

The course may focus on wafer handling (VDA 3.6 standard), generation of binary STDF test file and Wafermap.
*(**Provider: UL FE**, Duration: 20 hours, Level: Advanced)*

19. On Chip Die measurements

The course aims to provide an understanding of methods and equipment used for characterizing integrated circuits at the silicon die level. It covers the role of on-chip measurements in process validation, reliability assessment, and device modeling. Participants learn about the use of advanced measurement systems such as wafer probers, parameter analyzers, and RF instrumentation.
*(**Provider: UM FERI**, Duration: 20 hours, Level: Advanced)*

20. RISC-V bare metal programming

The "RISC-V Bare Metal Programming" workshop provides a hands-on introduction to low-level programming on RISC-V processors using the SiFive FE310 platform. Participants will learn how to write, compile, and run bare-metal applications directly on the hardware without an operating system. The workshop covers the fundamentals of RISC-V architecture, memory-mapped I/O, and interrupt handling using the Platform-Level Interrupt Controller (PLIC). Additionally, we will explore concepts of real-time task scheduling and how timing-sensitive operations can be implemented on such a lightweight RISC-V microcontroller.
*(**Provider: UL FRI,** Duration: 15 hours, Level: Advanced)*

21. RISC-V on FPGA

The "RISC-V on FPGA" workshop introduces participants to implementing and running a RISC-V processor on an FPGA, covering hardware synthesis, toolchain setup, and software execution on a custom soft-core CPU.
*(**Provider: UL FRI,** Duration: 20 hours, Level: Advanced)*

22. Organic semiconductors and devices

The participants will learn the basics of organic semiconductor materials as active materials in electronic devices. Next, the participants will have a hands-on training on the fabrication of an organic field-effect transistor. The training will combine deposition of organic semiconductor or semiconducting polymer, laser lithography (optional), and standard transconductance characterization of an organic field-effect transistor.
*(**Provider: UNG**, Duration: 30-40 hours, Level: Advanced)*

23. Two-dimensional semiconductors and devices

The participants will learn the basics of two-dimensional materials and their implementation in electronic devices. Next, the participants will have a hands-on training on the fabrication of a graphene-based field-effect transistor. The training will combine mechanical exfoliation of graphene, laser lithography, and basic current-voltage characterization of a graphene field-effect transistor.
*(**Provider: UNG**, Duration: 40 hours, Level: Advanced)*

24. OpenEDA - OpenLane DesignFlow

In this 3-to 4-day deep dive into OpenLane 2, participants will gain both theoretical understanding and hands-on experience with a complete open-source ASIC digital flow. We will begin with installation and environment setup, then step through the full design flow — from RTL through synthesis, placement & routing, timing closure, power optimization, and layout export — using real PDKs (such as SkyWater).
*(**Provider: UL FRI,** Duration: 3-4 days)*

25. Computer assisted circuit assembly (OpenEDA, ML/AI in chip design)

This course will guide you step by step in using a computer as a powerful tool for circuit design and prototyping. Through several modules, you'll gain both practical skills and new insights. First, you'll get familiar with the working environment and essential tools—Python, Visual Studio Code, PyOpus, and Spice. Then you'll learn how to prepare, simulate, and evaluate a circuit using Python. Finally, we'll introduce evolutionary algorithms and grammatical evolution, showing how they can guide your design process. Along the way, you'll also develop key skills such as defining grammatical rules and choosing objective functions to support innovative circuit design.
*(**Provider: UL FE**, Duration: 20-40 hours, Level: Basic)*

26. Basics of Chisel Hardware Construction Language

Chisel Hardware Construction Language is a domain specific language for designing synchronous digital circuits. It is an embedded language inside of the Scala programming language. It allows for more productive hardware circuit design by using metaprogramming features of Scala language. Chisel is conducive to describing hardware generators, i.e., programs that generate hardware based on given parameters. Such generators can than be used repeatdly by varying the parametrization and generate similar hardware. Advanced examples of hardware generators include: rocketchip - an SoC generation framework, chisel4ml - a generator of deeply quantized neural networks, FFT generator.

*(**Provider: IJS**, Duration: 40 hours, Level: Basic)*

27. Open source tools for schematic entry and circuit simulation (OpenEDA, ASIC design)

In this course, you will be introduced to the open-source schematic editor Xschem, used together with the powerful simulators Ngspice and VACASK. With Xschem, you'll not only create circuit schematics but also review your simulation results in an intuitive way. You'll also get a hands-on introduction to the NUTMEG scripting language built into Ngspice, giving you more control over simulations. Finally, we'll take a look at the IHP OpenPDK for the SG13G2 technology, opening the door to professional-grade design workflows.

*(**Provider: UL FE**, Duration: 20-40 hours, Level: Basic)*

28. TCL scripting

TCL is a widely used cross-platform scripting language that offers significant productivity benefits in engineering workflows. Its strengths in text processing, file manipulation, and system control make it an essential tool in electronic design automation (EDA). This course introduces the essential subset of the Tcl scripting language with a focus on its application in Xilinx Vivado. Through practical exercises, participants will learn how to run Vivado from scripts, automate design tasks, and extract key information from reports and source files, gaining hands-on experience with Tcl in an FPGA design environment.

*(**Provider: UL FRI,** Duration: 15 hours, Level: Advanced)*

29. EU level Supporting development - Graduate student professional training for technological progress advancement - internship

An invited seminar on selected topics provides listeners with insights from experts in the field.

*(**Provider: IJS,** Duration: 2 months - 96 hours of mentoring)*

PHOTONIC CHIPS

This section includes a list of training courses covering photonic integrated circuits (PICs), optical devices and tehnologies.

30. Basic course on photonic integration and PIC design

The course introduces photonic integrated circuits (PIC) and provides participants with motivation, basic knowledge about the integrated photonics, basic pasive and active components, operation principles, materials and applications. It is designed for anyone interested in the field of integrated photonics without any required previous knowledge on this particular topic. The course will generally cover basic passive and active components, material platforms, design, fabrication and testing of PICs. Specific focus of the course will be on applications of PICs and the oportunities provided through the fabless design approach. An overview of european (and worldwide) multi project wafer (MPW) services will also be made with the focus on oportunities for the industry.
*(**Provider: UL FE**, Duration: 20 hours, Level: Basic)*

31. Photonic integratied circuit design

The course will focus on the design of photonic integrated circuits (PIC) from concept to final layout. Participants will gain hands-on experience using professional software and workflow, including simulation, layout design and design rule check for fabrication. We will introduce two oposite yet complementary design flows typically used by PIC designers - component level design and circuit level design. Participants will gain experience in use of Lumerical software for component level simulations (MODE, EME and FDTD) as well as IPKISS and Klayout for circuit simulations and layout desing. Lab work presents the majority of this course. By the end of the course participants wil make their own designs that will be submitted for fabrication to a MPW fabrication service. The fabricated chip will be measured at UL and participants will recieve measurement results a few months after the end of the course.
*(**Provider: UL FE**, Duration: 40 hours, Level: Intermediate)*

32. Characterization and testing of photonic chips

This course will equip participants with first hand experience in characterization and testing of passive and active integrated photonic devices. The majority of the course will take place in a lab with hands on sessions using manual and automated setup for characterization of photonic integrated circuits (PIC). Participants will learn all the required steps that need to be taken to carry out accurate and repeatable optical and electro-optical measurements of PIC components and systems. Post processing and

analysis of measured data will also be carried out. Finally, participants wil also learn how to interpret the measurement results.
*(**Provider: UL FE**, Duration: 25 hours, Level: Advanced)*

33. Seminar on photonic integrated circuits and their applications

One day (couple of hours) seminar/webinar on a selected topic of photonic integrated circuits will present this cutting-edge technology and its main applications.
*(**Provider: UL FE**, Duration: 2-3 hours, Level: Basic)*

34. Seminar on quantum photonic integrated circits

One day (couple of hours) seminar/webnar on quantum photonic integrated circuits will present integrated photonics as a platform for quantum applications. Main advantages as well as challenges of this technology will be introduced.
*(**Provider: UL FE**, Duration: 2-3 hours, Level: Basic)*

35. Introduction to planar, channel waveguides and specialty optical fibres

This curse introduces basic principles, designs, manufacturing and applications of optical waveguides. The course will have a laboratory section demonstrating some devices and manufacturing processes.
*(**Provider: UM FERI**, Duration: 24 hours, Level: Basic)*

36. SiPM detector testing and usage

SiPM detectors are becoming the backbone for high tech systems relaying on photo detection to measure physical phenomenon, Lidar, Positron Emission Tomography, and Fluoresence, to name a few.
*(**Provider: IJS**, Duration: 1 - 3 months, 100- 44 hours , Level: Basic)*

37. Solid state photodetector technology overview

Daily seminar twice a year (SPAD arrays).
*(**Provider: IJS**, Duration: 5 hours, Level: Basic)*

QUANTUM CHIPS

This section includes a list of training courses covering quantum chips, superconducting devices, cryogenic measurements and hybrid device fabrication technologies.

38. Fundamentals of superconducting device fabrication

Course will provide training in fabrication of superconducting Josephson junction devices, which are the main building blocks of superconducting quantum processors, travelling wave parametric amplifiers, SFQ logic circuits and more.
*(**Provider: Nanocenter**, Duration: 40 hours, Level: Advanced)*

39. Characterization of superconducting devices

Course will provide training in sample preparation, cryogenic and vacuum system handling, and transport measurements at cryogenic temperatures. Course will cover basic 2-point and 4-point resistance measurements as well as advanced magnetoresistance measurements.
*(**Provider: Nanocenter**, Duration: 24 hours, Level: Advanced)*

40. Cryomemory device fundamentals

Course will provide basic knowledge on the novel type of cryomemory based on resistance switching in a correlated 2D material, showcasing its advanced characteristic. Course includes hands-on measurements at cryogenic temperatures.
*(**Provider: Nanocenter**, Duration: 40 hours, Level: Advanced)*

41. Hybrid devices - fabrication, test and measurement

Course will provide training in advanced fabrication of hybrid devices, which includes stacked heterostructure devices and superconducting/2D material devices. Fabrication will be performed in an inert atmosphere (i.e. glovebox), and measurements will be performed in a cryogenic chamber.
*(**Provider: Nanocenter**, Duration: 40 hours, Level: Advanced)*

SEMICONDUCTOR TECHNOLOGIES AND OTHER TOPICS

This section includes a list of training courses covering semiconductor materials, technologies including organic materials and other topics.

42. Introduction to thin film deposition (and related processes)

This entry level course will overview basic PVD and CVD thin film deposition process and equipment. The course will have a laboratory section demonstrating some equipment and device manufacturing.
*(**Provider: UM FERI**, Duration: 20 hours, Level: Basic)*

43. Nanofabrication

Course on nanofabrication will provide opportunity to learn the device fabrication techniques together with the associated control and characterization methods with the emphasis on hands on experience. Participants will get complete insight into the fabrication steps starting from the sample preparation and handling, preparation of the required CAD files and executables, use of e-beam lithographic patterning, thin film deposition, control of procedures using optical, SEM, FIB AFM, and similar characterization/analyses and electrical testing/measurements. The course will include advanced processing in controlled environments e.g. in inert glove-box atmosphere and vacuum.
*(**Provider: Nanocenter**, Duration: 40 hours, Level: Advanced)*

44. Laser lithography

Course will introduce principles of laser lithography, its advantages, limits and its application possibilities. It will offer hands-on experiece of lithographic patterning of the photoresist with the laser. At the end of the course individually trained students will be capable to perform the laser lithography independently.
*(**Provider: Nanocenter**, Duration: 20 hours, Level: Advanced)*

45. Hands-on training on Focused Ion Beam (FIB)

In the first step the trainees will learn the basics of scanning electron microscopy (SEM) and FIB operations. Trainees will learn how to make chips using FIB Pt deposition for scientific applications. Then they will learn how to perform electron beam lithography using FIB with nanometre precision for the preparation of chips. They will also learn how

to perform analysis of defects on chips with the cross-section technique. Defects will be thoroughly analysed using Energy-Dispersive X-Ray Spectroscopy (EDS) chemical analysis and with Scanning Transmission Electron Microscopy (STEM). For detailed 3-D analysis of samples on nanometre scale FIB tomography technique will be demonstrated. If there will be interest, also FIB lamella preparation training is also possible. The trainees will be able to use FIB during training under direct supervision of our instructors.
*(**Provider: Nanocenter**, Duration: 30 - 40 hours, Level: Advanced)*

46. Online workshop on Focused Ion Beam (FIB)

The participants will learn the basics of scanning electron microscopy (SEM) and FIB operations. They will learn about the FIB and SEM applications (cross-section analysis, analysis of defects on a chip, contact deposition, structure etching, 3D tomography, e-beam lithography, lamella fabrication…), and the limitations of the device. The workshop will be interactive, meaning the participants will be able to ask questions, and ask the operator to perform tasks they are most interested in.
*(**Provider: Nanocenter**, Duration: 8 hours, Level: Intermediate)*

47. Short course on chip-based micro and nano devices: design, manufacturing and applications

Short course on chip-based micro and nano devices: design, manufacturing and applications.
*(**Provider: UM FERI**)*

48. Secondary and primary school teachers - train the trainers

Selected topics of basic electronics, tailored to primary and secondary school teachers. Preparation of teaching course materials (videos, presentations, questionnaires), tools, and electronic components that will be used by teachers for their teaching activities.
*(**Provider: UL FE,** Duration: 20 hours, Level: Basic)*

49. IPR and TT internships

This short-term internship offers hands-on experience in technology transfer and intellectual property management offices. Participants will actively engage in patent drafting and filing, assessment of research results for innovation potential, preparation of licensing agreements, and evaluation of commercialisation opportunities. The aim is to provide a practical understanding of real-world TT and IPR processes through direct

mentorship and daily involvement in ongoing projects.
*(**Provider: IJS**, Duration: 80-160 hours, Level: Intermediate)*

50. Specialized training in technology transfer and IPR

This specialised course provides focused training on technology transfer processes and intellectual property rights (IPR) management. Participants will learn the fundamentals of patenting, IP protection strategies, licensing, and commercialisation of research results, as well as collaboration models between academia and industry. The course also offers optional follow-up consultations for participants who wish to discuss their specific cases or technology challenges in more detail.
*(**Provider: IJS**, Duration: 12 hours, Level: Intermediate)*

Information

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Slovenian Competence Centre on Chips and Semiconductor Technologies – CC Chip.si

Central hub for acceleration of development of chips and semiconductor technologies in Slovenia and Europe.

Learning for the future.

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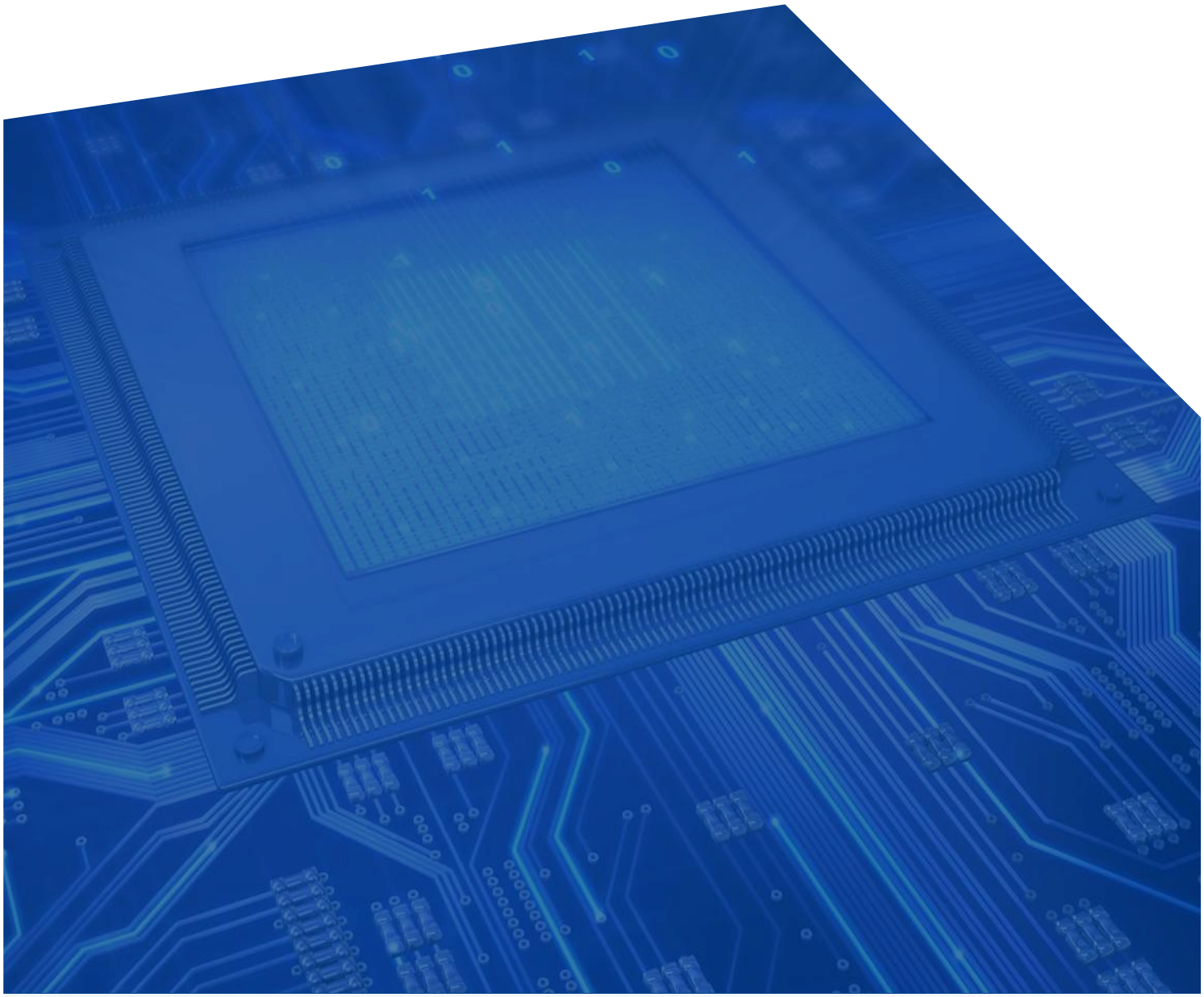

Chips JU

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MINISTRSTVO ZA DIGITALNO PREOBRAZBO

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